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MoS_2 for Enhanced Electrical Performance of Ultrathin Copper Films

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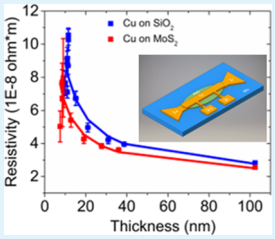
Supporting Information

ABSTRACT: Copper nanowires are widely used as on-chip interconnects due to their superior conductivity. However, with aggressive Cu interconnect scaling, surface scattering of electrons drastically increases the electrical resistivity. In this work, we have studied the electrical performance of Cu thin films deposited on different materials. By comparing the thickness dependence of Cu films' resistivity on MoS_2 and SiO_2, we have demonstrated that MoS_2 can be used to enhance the electrical performance of ultrathin Cu films due to improved specular surface scattering by up to 40%. By fitting the experimental data with the theoretical Fuchs−Sondheimer (FS) model, we have determined the specularity parameter at the Cu/MoS_2 interface to be $p \approx 0.4$ at room temperature. Furthermore, first principle calculations based on density functional theory (DFT) indicate that the localized density of states (LDOS) at the Cu/amorphous SiO_2 interface is larger than the LDOS at the Cu/MoS_2 interface, which is believed to be responsible for the higher resistivity in the Cu thin films that are deposited on SiO_2 substrates. Our results suggest that MoS_2 may serve as a performance enhancer for future generations of Cu interconnects.



KEYWORDS: *Cu interconnect, surface scattering, MoS_2 resistivity, FS model, DFT*

INTRODUCTION

Copper is widely used as interconnect material due to its superior conductivity.[1−4] Along with the scaling of VLSI circuits, scaling of interconnects is mandatory. Scaling trends of the height and width of those interconnects are discussed in the International Technology Roadmap for Semiconductors (ITRS).[4] However, when the thickness of Cu films decreases, reaching about the electron mean free path in copper, which is ∼40 nm at room temperature,[5] the electrical resistivity increases significantly due to increased electron scattering at the film surfaces[6−8] and grain boundaries.[9,10] This size effect impacts the time delay in interconnects severely and represents a major challenge.[3,4] Although pristine atomically smooth Cu surfaces show partially specular scattering,[11,12] there are many factors such as oxidation in ambient environment[10,13] or the coating with a secondary material[14] that can readily lead to diffusive surface scattering. Indeed, TaN/Ta bilayers have been used to encapsulate Cu interconnects in damascene structures as the diffusion barrier and liner layer to block Cu diffusion and provide good Cu adhesion.[15] However, it is well known that inelastic scattering at the Ta/Cu interface[14] can increase Cu resistivity due to wave function penetration. To address this problem, novel Cu/barrier interfaces exhibiting specular rather than diffusive electron scattering need to be developed to achieve highly conductive, ultrascaled interconnects.[11,13]

2D-layered materials have attracted substantial research interest for copper interconnect applications[13,16−20] due to their ultrathin body thickness. Recent studies show that an atomically thin layer of graphene not only blocks Cu diffusion efficiently[19,20] but can also enhance the electrical and thermal conductivity of Cu.[13] For example, Mehta et al.[13] reported partially specular scattering ($p = 0.23$) at a graphene-coated Cu surface. On the other hand, two-dimensional layered semiconducting transition metal dichalcogenides (TMDs) like MoS_2 have also shown to be good Cu diffusion barrier materials.[16] However, there exist only few studies on the electrical properties of Cu/MoS_2 interfaces.[18] Here, we have studied the electrical performance of Cu thin films on different material surfaces. Our experimental results show that for Cu films with the same thickness, Cu on MoS_2 always shows much lower resistivity compared to Cu on SiO_2. Analyzing the relation between Cu resistivity and thickness at different temperatures, we demonstrate that surface scattering is the main contribution to the total resistivity when Cu films are thinner than 40 nm, and the Cu/MoS_2 interface shows partially specular scattering with $p \approx 0.4$ at room temperature, which is better than that reported for Cu/Ni[11] and Cu/graphene[13] structures. Furthermore, we have studied the electronic properties of four different interfaces: pure Cu, Cu/amorphous SiO_2, Cu/crystalized SiO_2, and Cu/MoS_2 by first principle calculations based on density functional theory (DFT). Our findings are as follows: (1) the density of states (DOS) at the Cu/MoS_2 interface is similar to the pure Cu surface, and (2) the DOS of Cu/amorphous SiO_2 and Cu/crystalized SiO_2 is

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much higher than that of the Cu surface. It is worth mentioning that the DOS at the interfaces is localized, which we believe will trap electrons traversing near the interface. Upon subsequent release, the electron momentum will be randomized in the current direction. Thus, Cu located on SiO_2 can be expected to show higher resistivity than Cu on MoS_2 surfaces, since the highly localized DOS at the Cu/SiO_2 interface causes diffusive surface scattering. Our results indicate that Cu/MoS_2 hybrids have significantly improved electrical performance over Cu thin films with the same thickness, which is highly desirable for future generations of Cu interconnects.

RESULTS AND DISCUSSION

Two types of devices were fabricated: (i) Cu on MoS_2 and (ii) Cu on SiO_2, to study the electrical performance of Cu thin films on different materials. Figure 1a–d shows the schematic

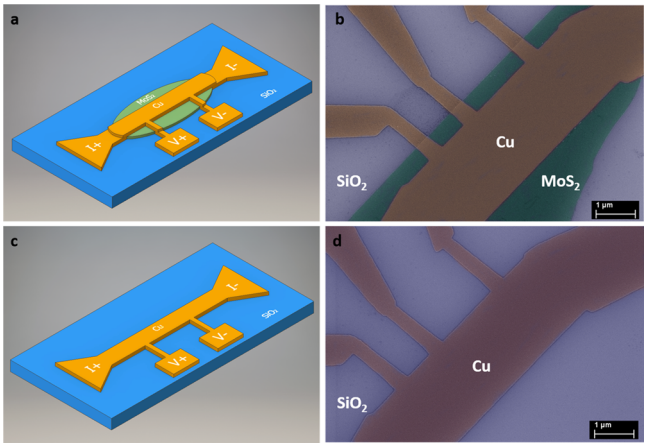

Figure 1. (a) Schematic diagram and (b) representative false-colored SEM image of a Cu on MoS_2 device. (c) Schematic diagram and (d) representative false-colored SEM image of a Cu on SiO_2 device.

diagrams and representative SEM images of a Cu/MoS_2 and a Cu/SiO_2 device, respectively. For a direct comparison, these two types of devices were patterned into structures with the same dimensions on the same Si/SiO_2 substrate (see Figure 1b,d). Cu thin films of different thicknesses were deposited using an e-beam evaporation system and the electrical resistance was measured by four-probe measurement in a probe station set-up. The measurement geometry is shown in Figure 1a,c. Details of the fabrication are described in the Methods section.

Before discussing the electrical performance, it is worthwhile taking a closer look at the actual material stacks. To study the various interfaces, cross-sectional structure and chemical analysis of both types of devices were carried out by scanning transmission electron microscopy (STEM). Energy dispersive X-ray spectroscopy (EDS) and electron energy loss spectroscopy (EELS) data along the respective blue arrows in Figure 2a,d are shown in Figure 2b,c,e,f. As apparent from all these data sets, an oxygen (O)-signal is consistently detected on the top surface of both devices. This signal is a result of Cu oxidation in air and occurs irrespective of what device type was studied. In addition, there is another O-signal at the Cu/SiO_2 interface as shown in Figure 2e,f. Note that in Figure 2e, the second O-signal (green circle) appeared simultaneously with the Si signal, while the O-signal at the upper Cu surface (black circle) does not coincide with a Si-signal, which is an indication that the second O-signal arises from SiO_2 rather than CuO_x. Moreover, no O-signal is detected at the Cu/MoS_2 interface. We conclude from these data that no CuO_x was formed during our copper deposition in vacuum at the lower interface but that oxidation occurred subsequently after removing the samples from the deposition chamber. The thickness of CuO_x measured from the blue dashed lines in Figure 2a–f is around 2.5 nm for both device types, and we have subtracted this value from all measured copper film thicknesses characterized by atomic force microscopy (AFM) to determine the actual Cu film thickness. Moreover, Cu deposited on MoS_2 and SiO_2 are both polycrystals as shown in Figure S2. The estimated average grain size for 7.5 and 102.5 nm Cu films deposited on MoS_2 are around 20 and 50 nm, respectively. For Cu deposited on SiO_2, the average grain size increases from 30 to 50 nm when the film thickness increases from 10 to 102.5 nm. According to a previous study by our group (see Figure S4 in the Supporting Information of ref 13), Cu thin films deposited on SiO_2 substrates using the same PVD e-beam evaporation system exhibit mainly a (111) grain orientation. At the same time, the annular bright field (ABF) images shown in Figure S3 indicate that also most of the Cu on MoS_2 has a preferential (111) grain orientation with a 2.08 Å interplanar spacing. Thus, in our study, Cu films deposited on MoS_2 and SiO_2 show the same crystallinity and grain structure.

Next, we analyze the electrical performance of Cu thin films on different materials. Figure 3a shows the resistivity of Cu on SiO_2 and Cu on MoS_2 as a function of the inverse of the Cu film thickness at room temperature. The symbols are experimental data, and the lines are theoretical fits employing the Fuchs–Sondheimer (FS) model and Mayadas–Shatzkes (MS) model (see eqs 1 and 2 below). Each data point represents the average resistivity obtained from more than 10 individual devices with the same Cu thickness employing a four-probe measurement approach. Similar resistance values were obtained when using a 400 μA DC current and a 10 μA AC current, which implies that the joule heating is negligible in our experiment. Comparing the resistivity of Cu on MoS_2 and SiO_2, we find that: (1) The resistivity of Cu increases as expected with decreasing Cu thickness, regardless of the underlying material. (2) The resistivity of Cu on MoS_2 is consistently smaller than that on SiO_2, and the thinner the Cu film, the larger the absolute difference between these two cases. It is worth noting that when Cu is 10 nm, the resistivity of Cu on MoS_2 is about 40% smaller than that on SiO_2. Compared with Cu films deposited on Si substrates from ref 8, Cu on SiO_2 in our work always shows higher resistivity even when the Cu layer is thicker than 100 nm. We attribute this to the lower quality of our evaporated Cu films if compared to the epitaxially grown Cu in ref 8. Interestingly, when the Cu thickness is less than 10 nm, the resistivity of Cu on MoS_2 is even much smaller than the reported results of epitaxial Cu on Si, as shown in Figure 3.

The first question arising from these findings is whether a material like MoS_2 with a much smaller bandgap than SiO_2 might act as a parallel conduction channel improving the effective conductivity of the stack. To this extent, we have fabricated back-gated MoS_2 transistors on the same substrate as shown in Figure 1. Figure S1 in the Supplementary Information shows typical subthreshold characteristics obtained from our devices. To conservatively evaluate the potential shunting through MoS_2, we are assuming that current levels may be as high as in the on-state (for high

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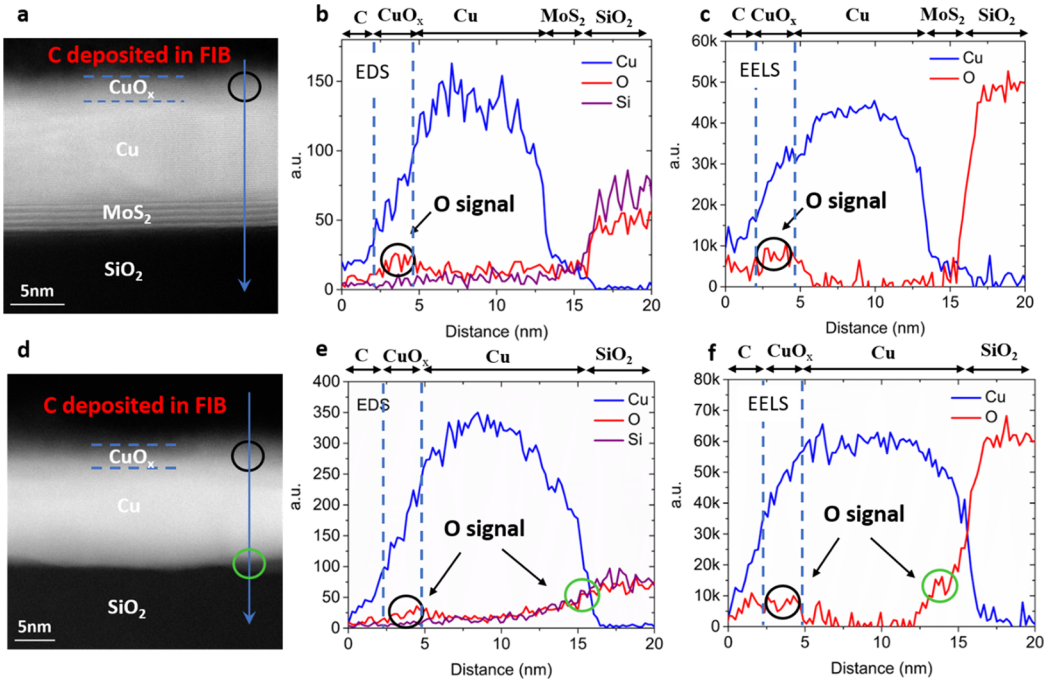

Figure 2. Cross-sectional STEM, EDS, and EELS line scan of a (a–c) Cu on MoS_2 and (d–f) Cu on SiO_2 device. The blue, red, and purple line represent the signal of Cu, O, and Si, respectively, along the blue arrow direction in (a) and (d). Note that a carbon (C) layer was deposited on top of both devices during the STEM sample preparation using focused ion beam (FIB) micromachining.

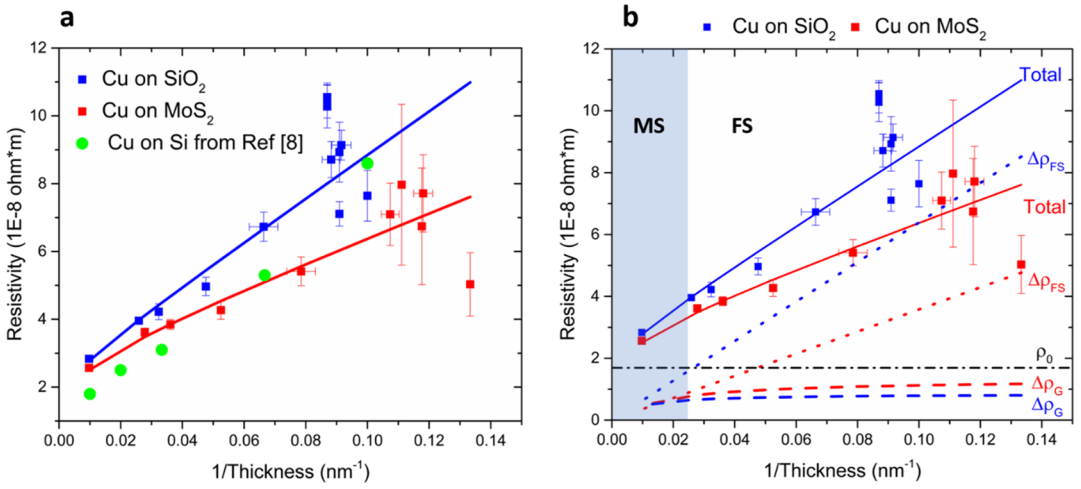

Figure 3. (a) Resistivity of Cu on SiO_2 and Cu on MoS_2 as a function of the inverse of the Cu film thickness at room temperature. Error bars capture the uncertainty in film thickness determination and resistivity calculation. The symbols are experimental data and the solid lines are fits using the FS and MS analytical models as discussed in the main text. The green dots are experimental data of Cu films on Si from ref 8. The dashed and dotted lines in (b) represent the resistivity increase due to grain boundary scattering and surface scattering of Cu on SiO_2 and MoS_2 calculated by the MS and FS equations, respectively. The dash-dotted line is the bulk resistivity of Cu.

positive gate voltages) of the device. For V_{ds} = 0.55 V, one can read out a normalized current of about I_d = 30 μA/μm in the device on-state, that is likely a vast overestimation of the MoS_2 contribution, considering that the Cu on MoS_2 hybrids are not gated. For the channel length and flake thickness noted in Figure S1 for this device a resistivity value of a few times 10^{-4} ohm·m can be extracted. Taking the dimensions of the flake into account, the resistance of MoS_2 is about four orders of magnitude higher than the resistance values for our hybrids. This implies that MoS_2 does not impact the resistivity of the stack significantly as a current shunt. Consequently, we conclude that the above-discussed improvement of resistivity in the case of Cu on MoS_2 is a result of modified scattering conditions in those copper films.

Contributions of surface scattering and grain boundary scattering to the total resistivity $\rho = \rho_0 + \Delta\rho_{FS} + \Delta\rho_G$ can be modeled by the Fuchs–Sondheimer (FS) eq 1[21] and the Mayadas–Shatzkes (MS) eq 2,[9] respectively,

$$\rho_{FS} = \rho_0 \left[1 + \frac{3}{2\kappa}(1-p)\int_1^\infty \left(\frac{1}{u^3} - \frac{1}{u^5}\right)\frac{1-e^{-\kappa u}}{1-pe^{-\kappa u}}du\right]^{-1} \quad (1)$$

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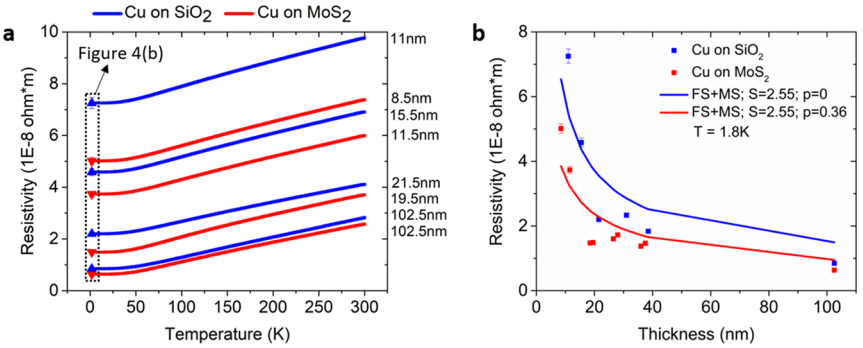

Figure 4. (a) Resistivity of Cu on SiO_2 and Cu on MoS_2 as a function of temperature for different Cu film thicknesses. (b) Resistivity of Cu on SiO_2 and Cu on MoS_2 as a function of the Cu film thickness at 1.8 K. The symbols are experimental data and the solid lines are fits obtained using the analytical FS and MS model. Error bars capture the uncertainty in numerical calculations and film thickness determination.

$$\rho_G = \rho_0\left[1 - \frac{3\alpha}{2} + 3\alpha^2 - 3\alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)\right]^{-1}$$
$$\text{where } \alpha = \frac{\Lambda_0}{d_{grain}}\left(\frac{R}{1-R}\right) \quad (2)$$

Here, ρ_0 is the bulk resistivity of Cu, $\kappa = t/\Lambda_0$, where Λ_0 is the electron mean free path, t is the thickness of the Cu film, p is the specularity parameter ranging from 0 (completely diffuse) to 1 (specular scattering), R is the grain-boundary reflection coefficient, and d_{grain} is the average grain size, which we assume to increase linearly with film thickness in our calculation. The increase in resistivity due to surface scattering and grain boundary scattering is thus given by $\Delta\rho_{FS} = \rho_{FS} - \rho_0$ and $\Delta\rho_G = \rho_G - \rho_0$, respectively.

In the FS model, for a relatively thick film or high temperature ($\kappa \gg 1$), eq 1 can be approximated by[21]

$$\rho_S = \rho_0\left[1 + \frac{3}{8}\frac{\Lambda_0}{t}(1-p)\right] \quad (3)$$

In contrast, for thin films or low temperature ($\kappa \ll 1$), eq 1 becomes[21]

$$\rho_S = \frac{4}{3}\frac{\rho_0\Lambda_0}{t\ln\left(\frac{\Lambda_0}{t}\right)}\frac{1-p}{1+p} \quad (4)$$

In our experiment, the thicknesses of Cu films range from 7.5 to 102.5 nm. At room temperature, the electron mean free path Λ_0 is 40 nm[5] and κ is between 0.19 to 2.6. Considering the small deviation of eq 3 from eq 1 (9% for $0.05 < \kappa < 1$)[22] and the large error bar in the experimental results for thin films (see Figure 3), eq 3 is appropriate to be used in our work to analyze surface scattering contributions at room temperature.

However, the FS model has limitations in explaining the dramatic increase in the resistivity for films less than 20 nm thick.[23−26] Rossnagel and Kuan[24] modified eq 3 by taking into account surface roughness through the introduction of an empirical factor S equal to or larger than 1:

$$\rho_S = \rho_0\left[1 + \frac{3}{8}\frac{S\Lambda_0}{t}(1-p)\right] \quad (5)$$

Next, we extract the grain-boundary reflection coefficient R and the numerical factor S by fitting the experimentally measured resistivity of Cu on SiO_2 using the reported Cu bulk resistivity value of $\rho_0 = 1.7\cdot10^{-8}$ Ωm[5]. Since the trap states at the Cu-oxide interface perturb the smooth surface potential of Cu,[14] we have assumed that electron scattering at both the Cu/CuO_x and Cu/SiO_2 interfaces is completely diffusive ($p = 0$), an approach that has been successfully applied by others.[8] Figure 3a shows the least square fit to our Cu on SiO_2 data as a solid blue line using eqs 2 and 5 with $R = 0.2$ and $S = 2.55$.

According to atomic force microscopy results, the surface roughness of Cu on MoS_2 is similar to that of Cu on SiO_2, and thus S is the same for both cases. Moreover, R should also be identical for both cases, since the Cu crystallinity is very similar as mentioned above. With all these parameters calibrated by our Cu on SiO_2 devices, we are in a position to determine "p", which was found to be $p = 0.44$ for the Cu/MoS_2 interface (see red line in Figure 3a). Figure 3b illustrates the resistivity increase due to grain boundary scattering and surface scattering in Cu on SiO_2 and MoS_2 devices as discussed above. As apparent from the figure, $\Delta\rho_G$varies slightly for the Cu thickness range from 102.5 to 7.5 nm, while $\Delta\rho_{FS}$increases by almost 10 times in the same thickness range. The figure also indicates, as expected, that the resistivity change for thick Cu films is mainly due to grain boundary scattering (light blue area in Figure 3b). On the other hand, surface scattering starts to dominate when the film thickness is smaller than the electron mean free path at room temperature. Our analysis also reveals that the resistivity difference between Cu on SiO_2 and Cu on MoS_2 devices mainly stems from surface scattering at the interfaces. Grain boundary scattering contributions between these two cases are similar.

To further substantiate our findings, we have studied the temperature dependence of scattering in Cu thin films. Figure 4a shows the experimentally measured resistivity of Cu on MoS_2 (red curves) and Cu on SiO_2 (blue curves) as a function of temperature ranging from 300 K to 1.8 K for a number of representative Cu films with different thicknesses. The measurements were carried out in a physical property measurement system (PPMS) using a lock-in set up with an AC current of 10 μA being applied. Each curve represents a set of experimental data obtained from one device. While the $\rho(T)$-dependence shows the expected saturation at low temperatures and a linear dependence for 50 K < T < 300 K due to phonon scattering (see refs 8, 27), it is interesting to note that: (i) within each set of the blue and red curves, the thicker Cu films always show a lower resistivity (irrespective of temperature) and (ii) for similar film thicknesses, the Cu resistivity on MoS_2 is always lower than the Cu resistivity on SiO_2, in agreement with our room-temperature findings. To extract "p" for low-temperatures, we have performed the same analysis as above using the FS and MS models. "p" was

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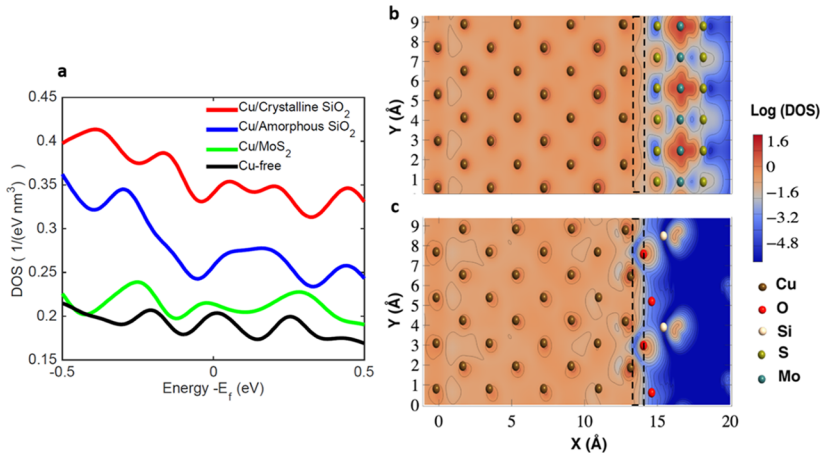

Figure 5. (a) DOS of Cu films with different interfaces integrated over the interface. The thickness of the interface is 1 angstrom. The interface volume is indicated in (b) and (c) by dashed line contours. The red, blue, green, and black lines correspond to the simulated interfaces between Cu and (i) crystalline SiO_2, (ii) amorphous SiO_2, (iii) MoS_2, and (iv) Cu interface with no passivated atoms, respectively. Projected density of states at the Fermi level energy for (b) Cu/MoS_2 and (c) Cu/amorphous SiO_2 interfaces, respectively.

assumed to be zero for the Cu on SiO_2 sample irrespective of temperature. $\rho_0\Lambda_0 = 6.7\cdot10^{-16}$ Ωm^2 was assumed to be independent of temperature,[28] since ρ_0 is inversely proportional to the temperature-dependent scattering time τ, while Λ_0 is proportional to τ. Since S represents the surface roughness contribution to the total resistivity, it is also independent of temperature. According to the reported studies (see Figure 1 in ref 29), the resistivity due to grain boundary scattering $\Delta\rho_G = \rho_G - \rho_0$ increases ~5% over the temperature range from 10 K to room temperature. Thus, the grain boundary scattering contribution at 1.8 K is calculated to be $\Delta\rho_{G\_1.8K} = \Delta\rho_{G\_300K}/1.05$. Since the electron mean free path $\Lambda_{0\_1.8K}$ is significantly larger than Λ_{0_300K}, eq 4 rather than eq 3 needs to be used to describe surface scatting contributions. Accordingly, the total resistivity at 1.8 K is calculated as:

$$\rho = \rho_{s\_1.8K} + \Delta\rho_{G\_1.8K} = \frac{4}{3}\frac{S\rho_0\Lambda_0}{t\ln\left(\frac{\Lambda_{0\_1.8K}}{t}\right)}\frac{1-p}{1+p} + \Delta\rho_{G\_300K}/1.05 \quad (6)$$

In Figure 4b, the symbols display the thickness dependence for the two types of devices at 1.8 K and the solid lines are fits obtained using the analytical FS and MS model. With all the assumptions discussed above, $\Lambda_{0\_1.8K}$ was determined to be 878 nm from the Cu on SiO_2 samples, which allowed extracting $p = 0.36$ for the Cu on MoS_2 samples. As apparent from Figure 4b, the deviation between the experimental and analytic fitting results is significant, which is due to the intrinsic limitations of the FS model, that is, in the limit of $\Lambda_0 \to \infty$, the vanishing bulk scattering leads to a vanishing thin film resistivity.[22] Thus, the extracted "p" value from our low-temperature data is in acceptable agreement with the p-value extracted at room temperature, considering that "p" should be temperature-independent according to the theoretical results reported by Zhou et al.[22] for temperature-independent elastic surface scattering.

To explain the underlying mechanism for the partially elastic surface scattering at the Cu/MoS_2 interface, we have carried out the first principle calculations based on density functional theory (DFT) to study the density of states impact at different Cu interfaces. It is worth mentioning that the DFT calculations are only used to qualitatively understand the interface effects through the local density of states, but not to calculate the resistivity shown in Figures 3 and 4, which corresponds to a large system. The details of the computational simulations are discussed in the Computational Details section. As shown in Figure 5a, the interface between Cu and MoS_2 has a similar DOS as the free Cu surface, while the interfaces between Cu and crystalline SiO_2 and amorphous SiO_2 exhibit a much higher DOS. The dashed areas in Figure 5b,c display the projected DOS at the interfaces of Cu/MoS_2 and Cu/amorphous SiO_2, respectively. The figure indicates that the DOS at the interface of Cu/MoS_2 is very small, which is consistent with the results shown in Figure 5a. However, at the interface of Cu/SiO_2, the DOS is large but not continuous (indicated by the blue parts in the dashed area). Considering that the DOS at the Cu/amorphous SiO_2 interface is higher than the one at the Cu/MoS_2 interface, we speculate that for electron propagation in thin Cu films, the probability of electrons being trapped at the Cu/amorphous SiO_2 interface is higher than at the Cu/MoS_2 interface. Upon subsequent release, the trapped electrons possess random momentum with regards to the current flow direction and thus effectively cause "p" to be zero, which is consistent with the studies in ref 30. Our observations are in general agreement with other publications that have demonstrated that the interaction between MoS_2 and Cu is very weak,[31] while the oxidation of the Cu surface or adsorption of foreign ad-atoms may cause perturbations to the Cu surface potential and effectively results in more surface scattering.[14,32]

CONCLUSIONS

In summary, we have studied the resistivity of Cu thin films on different materials and demonstrated that multilayer MoS_2 can be used to enhance the electrical performance of Cu. When the Cu film thickness is scaled down, the resistivity increases dramatically because of enhanced diffusive surface scattering. However, by adding an MoS_2 layer underneath the Cu film, the Cu resistivity can be significantly reduced due to partially specular surface scattering at the Cu/MoS_2 interface. From our analytic fitting results, we have extracted a specularity value of $p \approx 0.4$ at the Cu/MoS_2 interface at room temperature. According to our DFT calculations, the higher resistivity in

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Cu/SiO_2 is likely caused by the higher localized density of states (DOS) at the Cu/amorphous SiO_2 interface compared to the Cu/MoS_2 interface. While in our current experiments, only one surface of the Cu thin film was in contact with MoS_2, we expect further reduction in resistivity by coating MoS_2 on all Cu surfaces, which is highly desirable for future generations of Cu interconnects.

METHODS

Few-layer MoS_2 flakes were exfoliated onto Si/SiO_2 substrates followed by a 200 °C annealing step for 5 h in high vacuum. Subsequently, four probe test structures (4 μm length × 2 μm width) were fabricated on MoS_2 and SiO_2 surfaces with Cu thickness ranging from 7.5 to 102.5 nm, using e-beam lithography, e-beam evaporation metal deposition, and conventional lift-off processes. The thicknesses of the Cu films were measured using an atomic force microscope (AFM). The MoS_2 is in its 2H semiconducting phase as indicated by the Raman spectrum shown in Figure S4 and numerous electrical measurements on three-terminal device structures.

Computational Details. To quantify the effect of SiO_2 and MoS_2 on the charge distribution in copper, first principle calculations were carried out by density functional theory (DFT), using projector-argument waves (PAWs) as implemented in the VASP code.[33] In these calculations, the generalized-gradient approximation (GGA) with the Perdew-Burke-Ernzerhof (PBE) exchange-correlation functional were used.[33] In all the calculations, an energy cutoff of 500 eV with a convergence criterion of 1.0×10^{-8} eV and 0.1 eV $Å^{-1}$ for energies and forces, respectively, was used.

In this work, the Cu/SiO_2-cristobalite configuration corresponds to the simulated interface between Cu and cristobalite SiO_2. The configuration was constructed following the same process reported by Shan et al.[34] This interface was generated for copper oriented in the (001) direction, which was matched to α-cristobalite (001) with an in-plane strain value of 1.2%. Based on the work in ref 33, an oxygen-terminated interface was chosen since this type of termination has the strongest adhesion energy between both materials. To reduce the strain effects at the edges of the interface, eight atomic layers of each material were used in the x-direction as show in Figure 5b,c and only four layers on each side were relaxed while the rest of the atoms were fixed during the ionic relaxation.

Making use of the structure previously described, Cu on amorphous SiO_2 was also studied. The amorphous silica used in the interface region is prepared using the melt and quench method as suggested in ref 35. This process was carried out with the ReaxFF potential modified for the Cu/SiO_2 interface as reported in ref 36 in the large-scale atomic/molecular massive parallel simulation (LAMMPS).[37] During the molecular dynamics (MD) process, the copper atoms are fixed, and the atoms are annealed from 300 to 2000 K at a constant pressure for 200 ps to ensure a complete melting. Afterward, the structure is quenched using a stepwise cooling scheme at a rate of 12.5mK/fs and the structure is equilibrated at 300 K for an additional 10 ps and then relaxed in DFT, making use of the same parameters used for the Cu/SiO_2-cristobalite configuration. Finally, the Cu/MoS_2 interface is obtained by straining the MoS_2 atoms (the in-plane strain value is 0.34%) to match the Cu interface and then the supercell is relaxed following the same process as described for the SiO_2-cristobalite interface.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.9b03381.

Additional analysis on the resistivity of a back-gated MoS_2 transistor and additional information on the structures of MoS_2 and Cu films (PDF)

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Author Contributions

T.S. worked on the device fabrication, characterization, and data analysis. D.V., K.W., and M.P. worked on the DFT calculations. Z.C., J.A., and G.K. analyzed the data and oversaw the planning and execution of the project. Q.W. and M.K. worked on the structure analysis. T.S. wrote the manuscript.

Notes

The authors declare no competing financial interest.

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